M29DW324DT
M29DW324DB

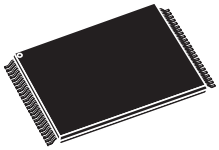
32 Mbit (4Mb x8 or 2Mb x16, Dual Bank, Boot Block) 3V Supply Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V for Program, Erase and Read
  - V_{PP} =12V for Fast Program (optional)
- ACCESS TIME: 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte/Word typical
  - Double Word/ Quadruple Byte Program
- MEMORY BLOCKS
  - Dual Bank Memory Array: 16+16 Mbit
  - Parameter Blocks (Top or Bottom Location)
- DUAL OPERATIONS
  - Read in one bank while Program or Erase in other
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- $V_{PP}/\overline{WP}$ PIN for FAST PROGRAM and WRITE PROTECT
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- EXTENDED MEMORY BLOCK
  - Extra block used as security block or to store additional information
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Top Device Code M29DW324DT: 225Ch
  - Bottom Device Code M29DW324DB: 225Dh

Figure 1. Packages



TSOP48 (N)
12 x 20mm

TFBGA63 (ZA)
63 ball array

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SUMMARY DESCRIPTION

The M29DW324D is a 32 Mbit (4Mb x8 or 2Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The device features an asymmetrical block architecture. The M29DW324D has an array of 8 parameter and 63 main blocks and is divided into two Banks, A and B, providing Dual Bank operations. While programming or erasing in Bank A, read operations are possible in Bank B and vice versa. Only one bank at a time is allowed to be in program or erase mode. The bank architecture is summarized in Table 2. M29DW324DT locates the Parameter Blocks at the top of the memory address space while the M29DW324DB locates the Parameter Blocks starting from the bottom.

M29DW324D has an extra 64KByte block (Extended Block) that can be accessed using a dedicated command. The Extended Block can be protected and so is useful for storing security information. However the protection is irreversible, once protected the protection cannot be undone.

Each block can be erased independently so it is possible to preserve valid data while old data is erased. The blocks can be protected to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12x20mm) and TFBGA63 (7x11mm, 0.8mm pitch) packages. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

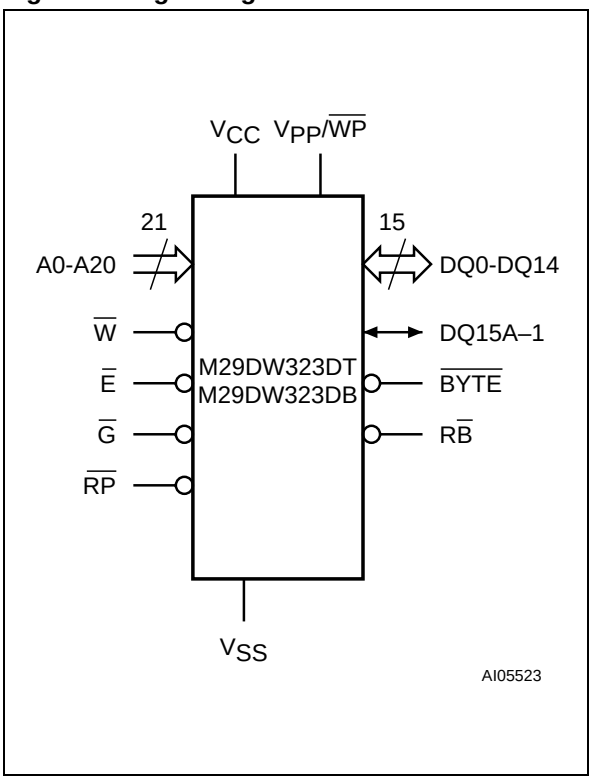


Table 1. Signal Names

A0-A20	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A–1	Data Input/Output or Address Input
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
$\overline{BYTE}$	Byte/Word Organization Select
V_{CC}	Supply Voltage
$V_{PP}/\overline{WP}$	V_{PP}/Write Protect
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

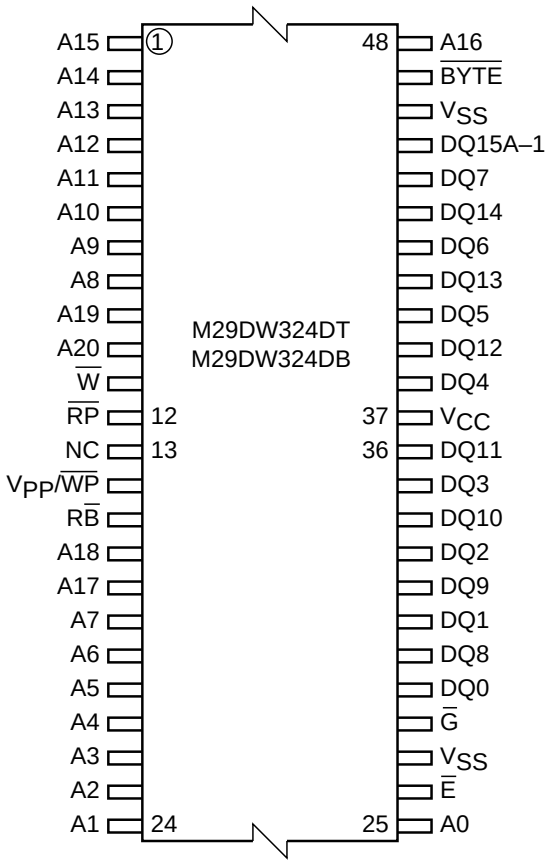
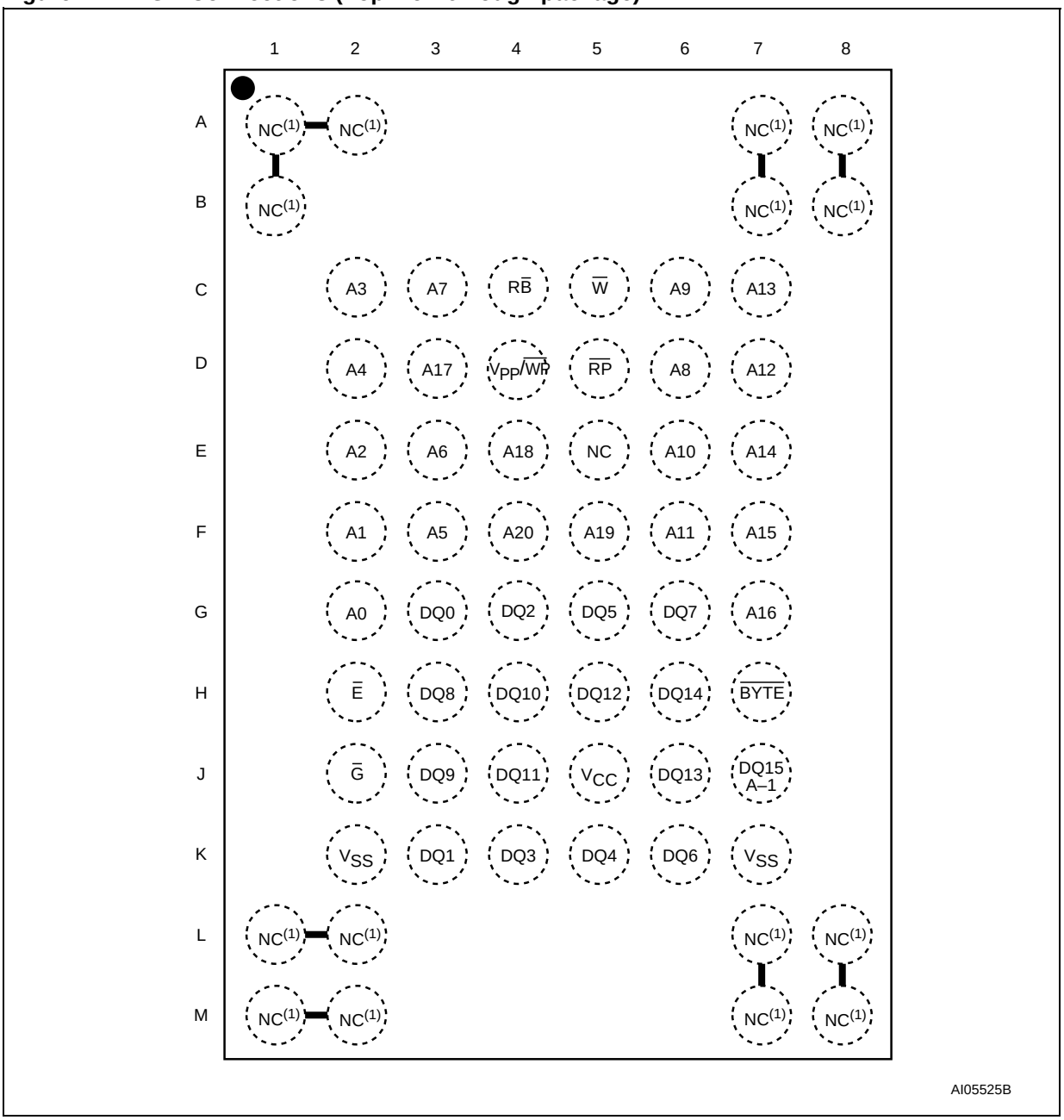


Figure 4. TFBGA Connections (Top view through package)

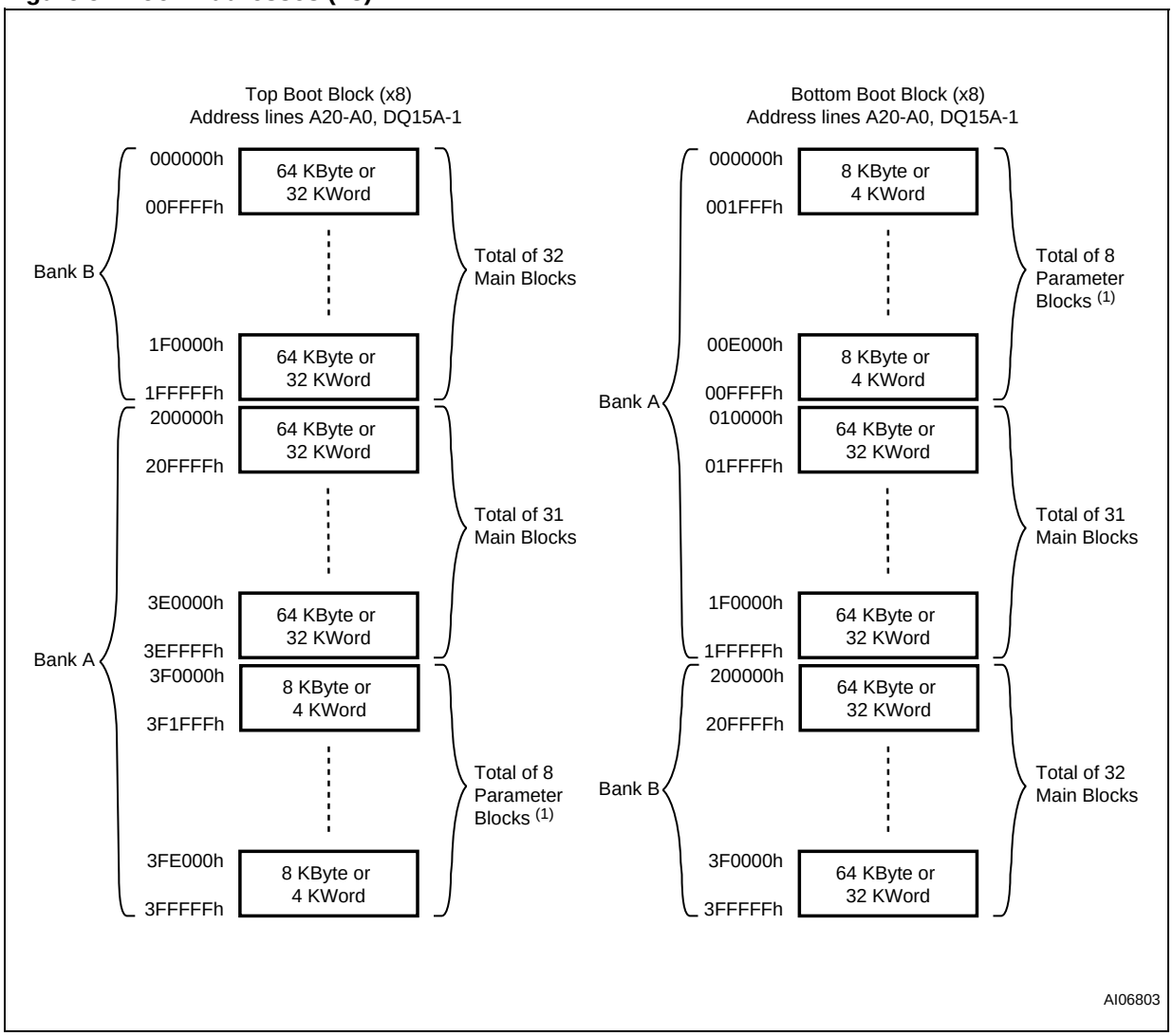


Note: 1. Balls are shorted together via the substrate but not connected to the die.

Table 2. Bank Architecture

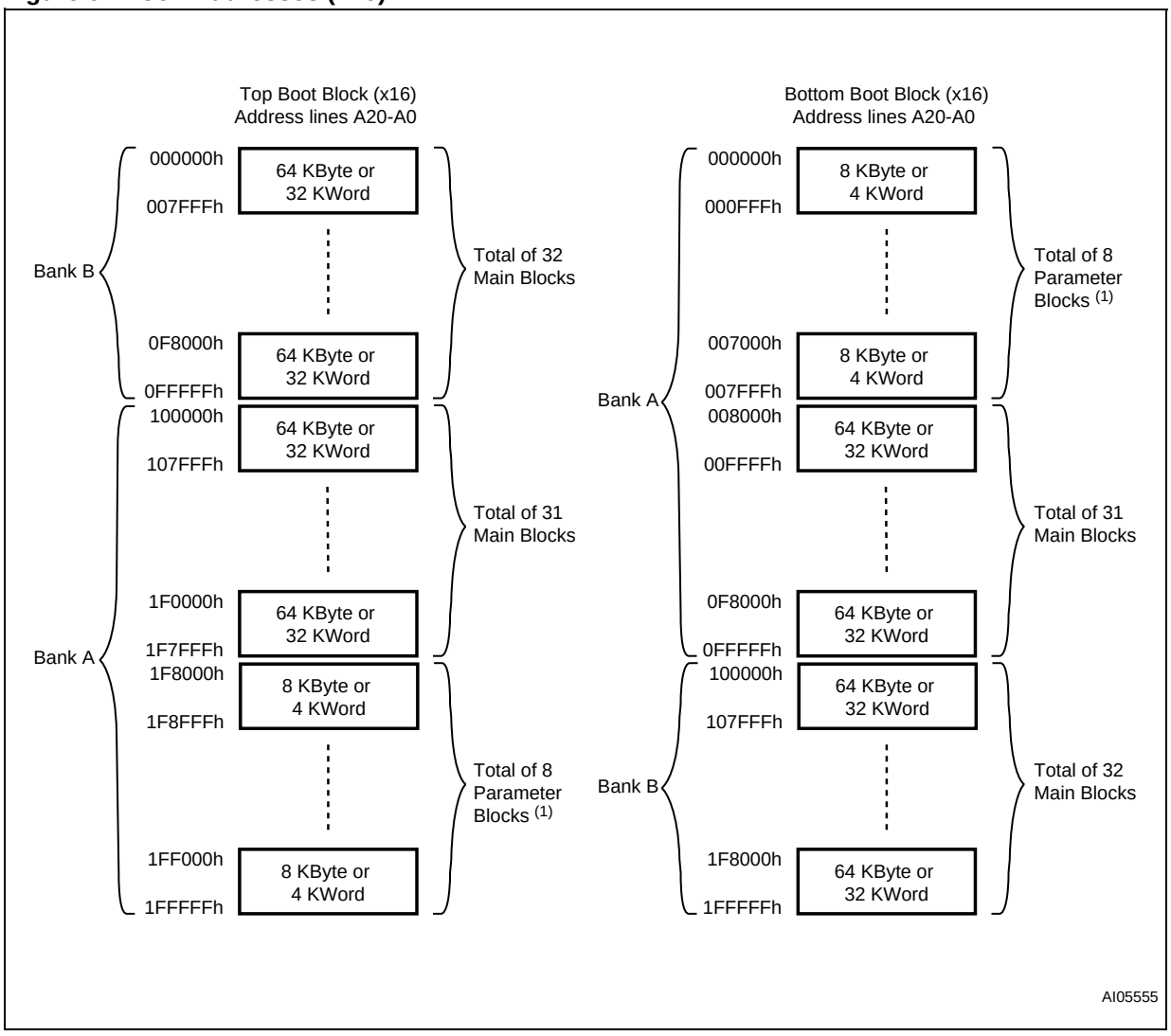
Bank	Bank Size	Parameter Blocks		Main Blocks	
		No. of Blocks	Block Size	No. of Blocks	Block Size
A	16 Mbit	8	8KByte/ 4 KWord	31	64KByte/ 32 KWord
B	16 Mbit	-		32	64KByte/ 32 KWord

Figure 5. Block Addresses (x8)



Note: 1. Used as Extended Block Addresses in Extended Block mode.
2. Also see Appendix A, Tables 19 and 20 for a full listing of the Block Addresses.

Figure 6. Block Addresses (x16)



Note: 1. Used as Extended Block Addresses in Extended Block mode.
2. Also see Appendix A, Tables 19 and 20 for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ0-DQ7). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ8-DQ14). The Data I/O outputs the data stored at the selected address during a Bus Read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During Bus Write operations the Command Register does not use these bits. When reading the Status Register these bits should be ignored.

Data Input/Output or Address Input (DQ15A–1). When $\overline{BYTE}$ is High, V_{IH}, this pin behaves as a Data Input/Output pin (as DQ8-DQ14). When $\overline{BYTE}$ is Low, V_{IL}, this pin behaves as an address pin; DQ15A–1 Low will select the LSB of the addressed Word, DQ15A–1 High will select the MSB. Throughout the text consider references to the Data Input/Output to include this pin when $\overline{BYTE}$ is High and references to the Address Inputs to include this pin when $\overline{BYTE}$ is Low except when stated explicitly otherwise.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

V_{PP}/Write Protect ($V_{PP}/\overline{WP}$). The V_{PP}/Write Protect pin provides two functions. The V_{PP} function allows the memory to use an external high voltage power supply to reduce the time required for Program operations. This is achieved by bypassing the unlock cycles and/or using the Double Word or Quadruple Byte Program commands. The Write Protect function provides a hardware method of protecting the two outermost boot blocks.

When V_{PP}/Write Protect is Low, V_{IL}, the memory protects the two outermost boot blocks; Program and Erase operations in these blocks are ignored while V_{PP}/Write Protect is Low, even when $\overline{RP}$ is at V_{ID}.

When V_{PP}/Write Protect is High, V_{IH}, the memory reverts to the previous protection status of the two outermost boot blocks. Program and Erase operations can now modify the data in these blocks unless the blocks are protected using Block Protection.

When V_{PP}/Write Protect is raised to V_{PP} the memory automatically enters the Unlock Bypass mode. When V_{PP}/Write Protect returns to V_{IH} or V_{IL} normal operation resumes. During Unlock Bypass Program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the Command Interface section. The transitions from V_{IH} to V_{PP} and from V_{PP} to V_{IH} must be slower than t_{VHVPP}, see Figure 15.

Never raise V_{PP}/Write Protect to V_{PP} from any mode except Read mode, otherwise the memory may be left in an indeterminate state.

The V_{PP}/Write Protect pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP}/Write Protect pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

Reset/Block Temporary Unprotect ($\overline{RP}$). The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

Note that if $V_{PP}/\overline{WP}$ is at V_{IL}, then the two outermost boot blocks will remain protected even if RP is at V_{ID}.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, Table 16 and Figure 14, Reset/Temporary Unprotect AC Characteristics for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

Ready/Busy Output ($\overline{RB}$). The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-im-

pedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See Table 16 and Figure 14, Reset/Temporary Unprotect AC Characteristics.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Byte/Word Organization Select ($\overline{BYTE}$). The Byte/Word Organization Select pin is used to switch between the x8 and x16 Bus modes of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

V_{CC} Supply Voltage (2.7V to 3.6V). V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Program and Erase operations, I_{CC3}.

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby.

The Dual Bank architecture of the M29DW324D allows read/write operations in Bank A, while read operations are being executed in Bank B or vice versa. Write operations are only allowed in one bank at a time.

See Tables 3 and 4, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 11, Read Mode AC Waveforms, and Table 13, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 12 and 13, Write AC Waveforms, and Tables 14 and 15, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 12, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Tables 3 and 4, Bus Operations.

Block Protect and Chip Unprotect. Groups of blocks can be protected against accidental Program or Erase. The Protection Groups are shown in Appendix A, Tables 19 and 20, Block Addresses. The whole chip can be unprotected to allow the data inside the blocks to be changed.

The V_{PP}/Write Protect pin can be used to protect the two outermost boot blocks. When V_{PP}/Write Protect is at V_{IL} the two outermost boot blocks are protected and remain protected regardless of the Block Protection Status or the Reset/Block Temporary Unprotect pin status.

Block Protect and Chip Unprotect operations are described in Appendix C.

Table 3. Bus Operations, $\overline{BYTE} = V_{IL}$

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs DQ15A–1, A0-A20	Data Inputs/Outputs	
					DQ14-DQ8	DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Hi-Z	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Hi-Z	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	20h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	Hi-Z	5Ch (M29DW324DT) 5Dh (M29DW324DB)

Note: X = V_{IL} or V_{IH}.

Table 4. Bus Operations, $\overline{BYTE} = V_{IH}$

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A20	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	0020h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	225Ch (M29DW324DT) 225Dh (M29DW324DB)

Note: X = V_{IL} or V_{IH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode. See either Table 5, or 6, depending on the configuration that is being used, for a summary of the commands.

Read/Reset Command.

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the timeout of a Block erase operation then the memory will take up to 10µs to abort. During the abort period no valid data can be read from the memory. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

Auto Select Command.

The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. It can be addressed to either Bank. Three consecutive Bus Write operations are required to issue the Auto Select command. The final Write cycle must be addressed to one of the Banks. Once the Auto Select command is issued Bus Read operations to the Bank where the command was issued output the Auto Select data. Bus Read operations to the other Bank will output the contents of the memory array. The memory remains in Auto Select mode until a Read/Reset or CFI Query command is issued.

In Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL} and A18-A20 = Bank Address. The other address bits may be set to either V_{IL} or V_{IH}.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL} and A18-A20 = Bank Address. The other address bits may be set to either V_{IL} or V_{IH}.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, A18-A20 = Bank Address and A12-A17 specifying the address of the block inside the Bank. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

Read CFI Query Command.

The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. This command is valid when the device is in the Read Array mode, or when the device is in Autoselected mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Autoselected mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Autoselected mode.

See Appendix B, Tables 21, 22, 23, 24, 25 and 26 for details on the information contained in the Common Flash Interface (CFI) memory area.

Program Command.

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. After programming has started, Bus Read operations in the Bank being programmed output the Status Register content, while Bus Read operations to the other Bank output the contents of the memory array. See the section on the Status Register for more details. Typical program times are given in Table 7.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Fast Program Commands

There are two Fast Program commands available to improve the programming throughput, by writing several adjacent words or bytes in parallel. The Quadruple Byte Program command is available for x8 operations, while the Double Word Program command is available for x16 operations.

Quadruple Byte Program Command. The Quadruple Byte Program command is used to write a page of four adjacent Bytes in parallel. The four bytes must differ only for addresses A0, DQ15A-1. Five bus write cycles are necessary to issue the Quadruple Byte Program command.

- The first bus cycle sets up the Quadruple Byte Program Command.
- The second bus cycle latches the Address and the Data of the first byte to be written.
- The third bus cycle latches the Address and the Data of the second byte to be written.
- The fourth bus cycle latches the Address and the Data of the third byte to be written.
- The fifth bus cycle latches the Address and the Data of the fourth byte to be written and starts the Program/Erase Controller.

Double Word Program Command. The Double Word Program command is used to write a page of two adjacent words in parallel. The two words must differ only for the address A0.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Only one bank can be programmed at any one time. The other bank must be in Read mode or Erase Suspend.

Programming should not be attempted when V_{PP} is not at V_{PPH}.

After programming has started, Bus Read operations in the Bank being programmed output the Status Register content, while Bus Read operations to the other Bank output the contents of the memory array.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Fast Program commands cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Typical Program times are given in Table 7, Program, Erase Times and Program/Erase Endurance Cycles.

Unlock Bypass Command.

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the bank enters Unlock Bypass mode. The Unlock Bypass Program command can then be issued to program addresses within the bank, or the Unlock Bypass Reset command can be issued to return the bank to Read mode. In Unlock Bypass mode the memory can be read as if in Read mode.

When V_{PP} is applied to the V_{PP}/Write Protect pin the memory automatically enters the Unlock Bypass mode and the Unlock Bypass Program command can be issued immediately.

Unlock Bypass Program Command.

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. The operation cannot be aborted, a Bus Read operation to the Bank where the command was issued outputs the Status Register. See the Program command for details on the behavior.

Unlock Bypass Reset Command.

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass Mode.

Chip Erase Command.

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the

blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 7. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

Block Erase Command.

The Block Erase command can be used to erase a list of one or more blocks in a Bank. It sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. All blocks must belong to the same Bank; if a block belonging to the other Bank is given it will not be erased. The Block Erase operation starts the Program/Erase Controller after a time-out period of 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. After the sixth Bus Write operation a Bus Read operation within the same Bank will output the Status Register. See the Status Register section for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the 50µs time-out period. Typical block erase times are given in Table 7.

After the Erase operation has started all Bus Read operations to the Bank being erased will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs Bus Read operations to the Bank where the command was issued will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Erase Suspend Command.

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within 50 µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

During Erase Suspend a Bus Read operation to the Extended Block will output the Extended Block data.

Erase Resume Command.

The Erase Resume command must be used to restart the Program/Erase Controller after an Erase Suspend. The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

Enter Extended Block Command

The M29DW324D has an extra 64KByte block (Extended Block) that can only be accessed using the Enter Extended Block command. Three Bus write cycles are required to issue the Extended Block command. Once the command has been issued the device enters Extended Block mode where all Bus Read or Write operations to the Boot Block addresses access the Extended Block. Therefore in Extended Block mode the Boot Blocks are not accessible. In Extended Block mode dual operations are possible, with the Extended Block mapped in Bank A. All commands are accepted by the command interface.

To exit from the Extended Block mode the Exit Extended Block command must be issued.

The Extended Block can be protected, however once protected the protection cannot be undone.

Exit Extended Block Command.

The Exit Extended Block command is used to exit from the Extended Block mode and return the device to Read mode. Four Bus Write operations are required to issue the command.

Block Protect and Chip Unprotect Commands.

Groups of blocks can be protected against accidental Program or Erase. The Protection Groups are shown in Appendix A, Tables 19 and 20, Block Addresses. The whole chip can be unprotected to allow the data inside the blocks to be changed.

Block Protect and Chip Unprotect operations are described in Appendix C.

Table 5. Commands, 16-bit mode, $\overline{BYTE}$ = V_{IH}

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	(BKA) 555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Double Word Program	3	555	50	PA0	PD0	PA1	PD1						
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	BKA	B0										
Erase Resume	1	BKA	30										
Read CFI Query	1	55	98										
Enter Extended Block	3	555	AA	2AA	55	555	88						
Exit Extended Block	4	555	AA	2AA	55	555	90	X	00				

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block, BKA Bank Address. All values in the table are in hexadecimal.

The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A20, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 6. Commands, 8-bit mode, $\overline{BYTE}$ = V_{IL}

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset	1	X	F0										
	3	AAA	AA	555	55	X	F0						
Auto Select	3	AAA	AA	555	55	(BKA) AAA	90						
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Quadruple Byte Program	5	AAA	55	PA0	PD0	PA1	PD1	PA2	PD2	PA3	PD3		
Unlock Bypass	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase	6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BA	30
Erase Suspend	1	BKA	B0										
Erase Resume	1	BKA	30										
Read CFI Query	1	AA	98										
Enter Extended Block	3	AAA	AA	555	55	AAA	88						
Exit Extended Block	4	AAA	AA	555	55	AAA	90	X	00				

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal. The Command Interface only uses A–1, A0-A10 and DQ0-DQ7 to verify the commands; A11-A20, DQ8-DQ14 and DQ15 are Don't Care. DQ15A–1 is A–1 when $\overline{BYTE}$ is V_{IL} or DQ15 when $\overline{BYTE}$ is V_{IH}.

Table 7. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1)	Typical after 100k W/E Cycles (1)	Max	Unit
Chip Erase		40	40	200	s
Block Erase (64 KBytes)		0.8		6	s
Program (Byte or Word)		10		200	µs
Double Word Program (Byte or Word)		10		200	µs
Chip Program (Byte by Byte)		40		200	s
Chip Program (Word by Word)		20		100	s
Chip Program (Quadruple Byte or Double Word)		10		100	s
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. T_A = 25°C, V_{CC} = 3.3V.

STATUS REGISTER

The M29DW324D has two Status Registers, one for each bank. The Status Registers provide information on the current or previous Program or Erase operations executed in each bank. The various bits convey information and errors on the operation. Bus Read operations from any address within the Bank, always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in Table 8, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 7, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 8, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 8. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RB
Program	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program During Erase Suspend	Bank Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program Error	Bank Address	$\overline{DQ7}$	Toggle	1	–	–	0
Chip Erase	Bank Address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	1
	Non-Erasing Block	Data read as normal					1
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle	0
	Faulty Block Address	0	Toggle	1	1	Toggle	0

Note: Unspecified data bits should be ignored.

Figure 7. Data Polling Flowchart

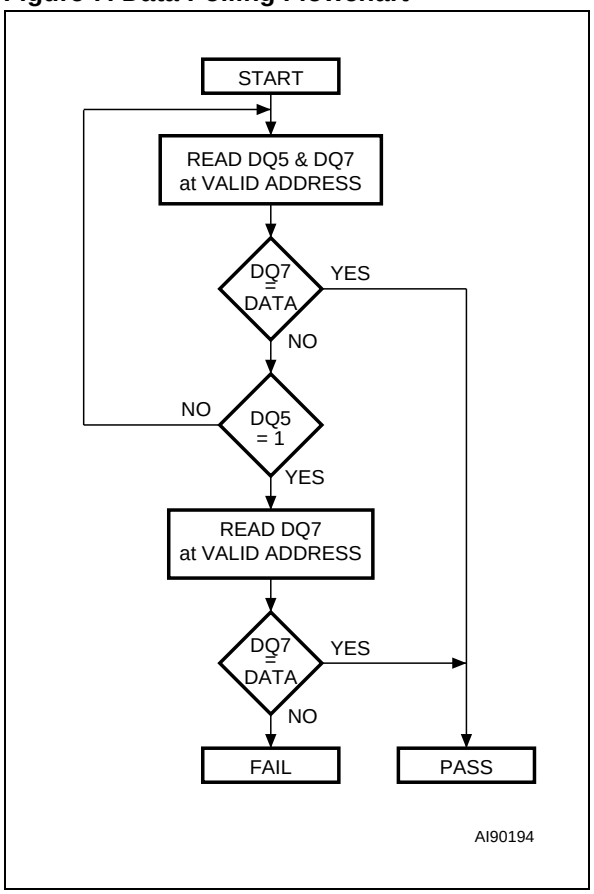
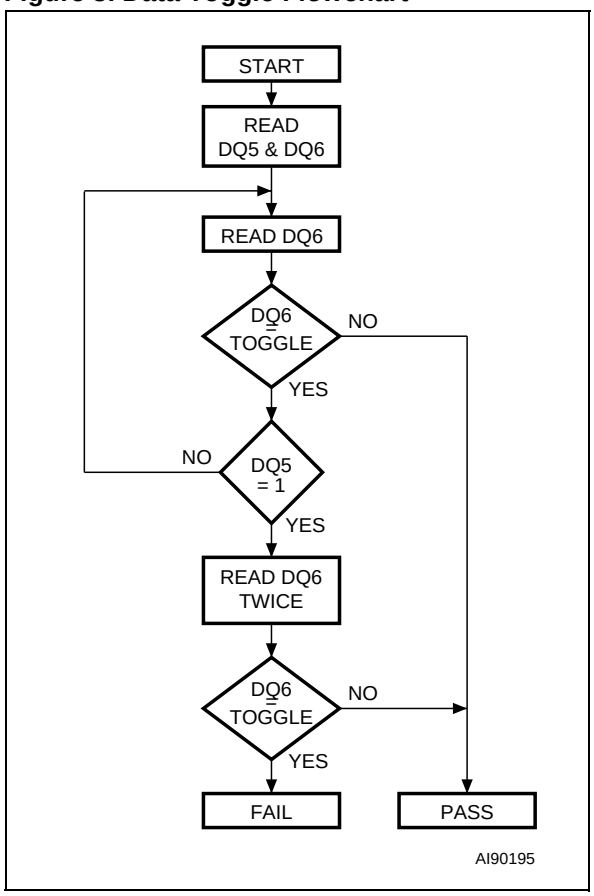


Figure 8. Data Toggle Flowchart



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage (1,2)	–0.6	V_{CC} +0.6	V
V_{CC}	Supply Voltage	–0.6	4	V
V_{ID}	Identification Voltage	–0.6	13.5	V
V_{PP}(3)	Program Voltage	–0.6	13.5	V

Note: 1. Minimum voltage may undershoot to –2V during transition and for less than 20ns during transitions.
2. Maximum voltage may overshoot to V_{CC} +2V during transition and for less than 20ns during transitions.
3. V_{PP} must not remain at 12V for more than a total of 80hrs.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 10, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 10. Operating and AC Measurement Conditions

Parameter	M29DW324D				Unit
	70		90		
	Min	Max	Min	Max	
V_{CC} Supply Voltage	3.0	3.6	2.7	3.6	V
Ambient Operating Temperature	–40	85	–40	85	°C
Load Capacitance (C_L)	30		30		pF
Input Rise and Fall Times		10		10	ns
Input Pulse Voltages	0 to V_{CC}		0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 9. AC Measurement I/O Waveform

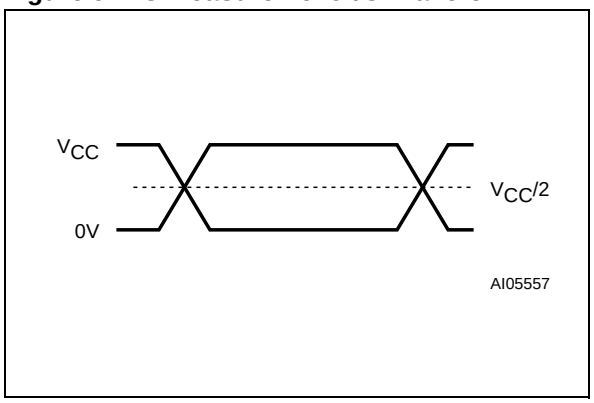


Figure 10. AC Measurement Load Circuit

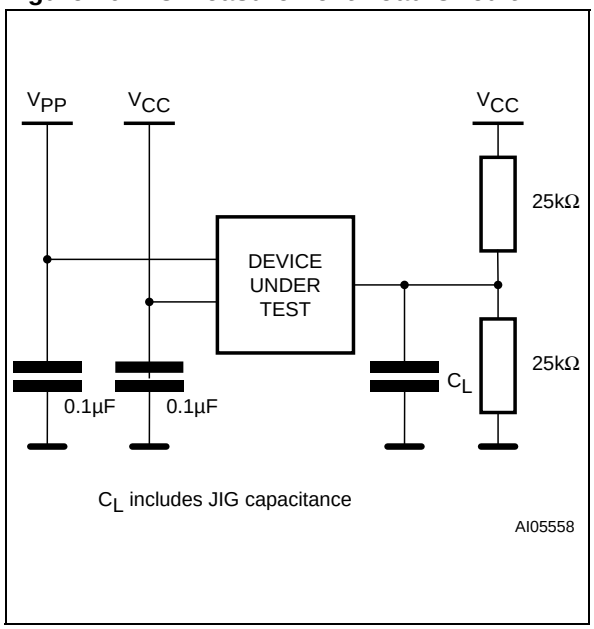


Table 11. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 12. DC Characteristics

Symbol	Parameter	Test Condition		Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}(2)	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz			10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$			100	µA
I_{CC3} (1,2)	Supply Current (Program/ Erase)	Program/Erase Controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}		20	mA
			$V_{PP}/\overline{WP} = V_{PP}$		20	mA
V_{IL}	Input Low Voltage			–0.5	0.8	V
V_{IH}	Input High Voltage			$0.7V_{CC}$	V_{CC} +0.3	V
V_{PP}	Voltage for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 3.0V ±10%		11.5	12.5	V
I_{PP}	Current for $V_{PP}/\overline{WP}$ Program Acceleration	V_{CC} = 3.0V ±10%			15	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100µA		V_{CC} –0.4		V
V_{ID}	Identification Voltage			11.5	12.5	V
I_{ID}	Identification Current	$A9 = V_{ID}$			100	µA
V_{LKO}	Program/Erase Lockout Supply Voltage			1.8	2.3	V

Note: 1. Sampled only, not 100% tested.
2. In Dual operations the Supply Current will be the sum of I_{CC1}(read) and I_{CC3} (program/erase).

Figure 11. Read Mode AC Waveforms

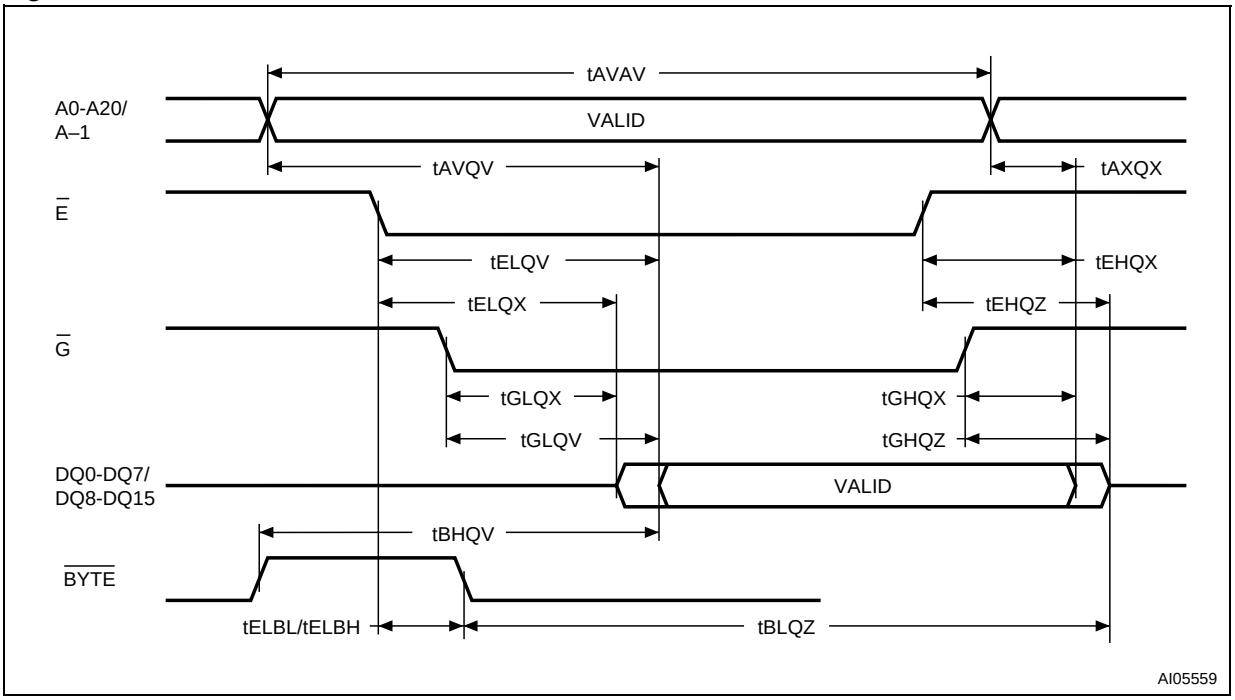


Table 13. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29DW324D		Unit
					70	90	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Min	70	90	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	Max	70	90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}	Max	70	90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}	Max	30	35	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	Max	25	30	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	Max	25	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	30	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	40	ns

Note: 1. Sampled only, not 100% tested.

Figure 12. Write AC Waveforms, Write Enable Controlled

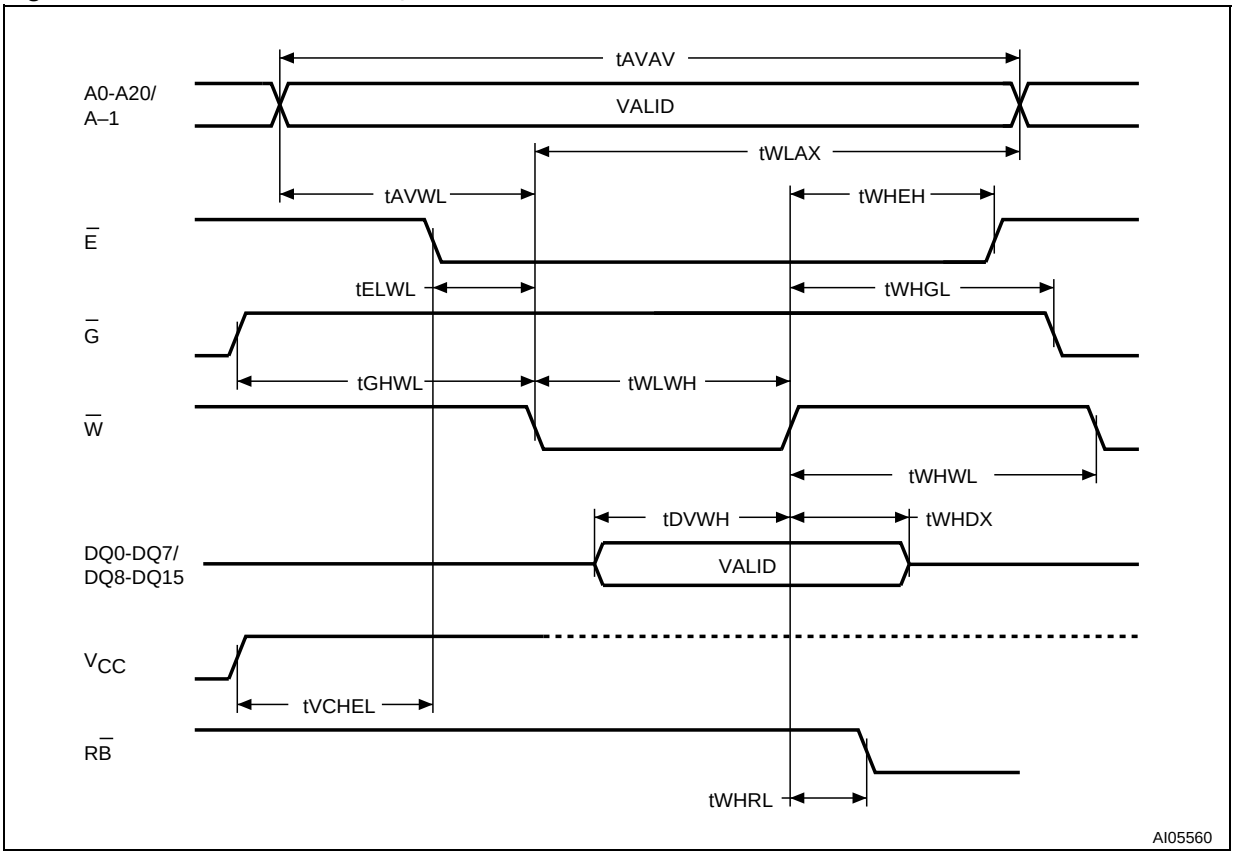


Table 14. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M29DW324D		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	50	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	50	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	50	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	35	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

Note: 1. Sampled only, not 100% tested.

Figure 13. Write AC Waveforms, Chip Enable Controlled

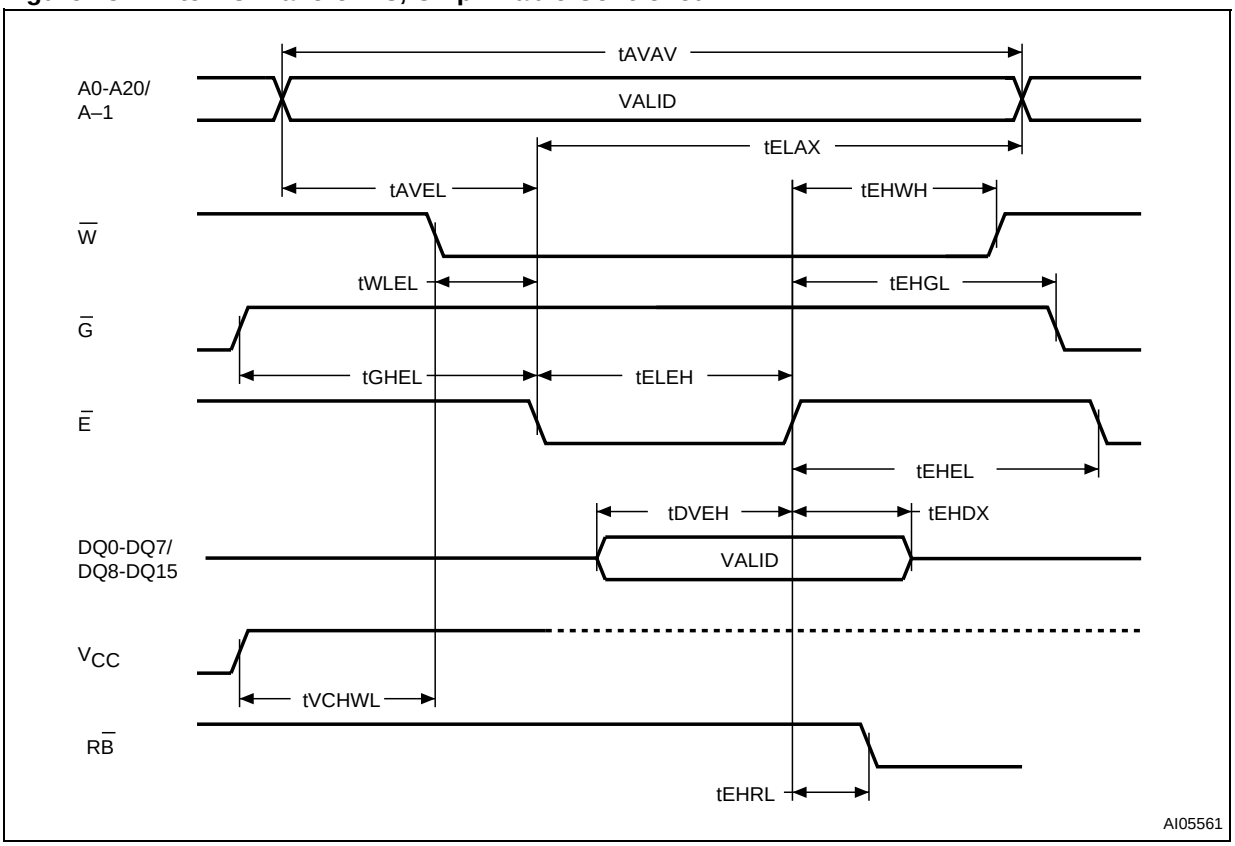


Table 15. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M29DW324D		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	50	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	50	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	50	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	35	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

Note: 1. Sampled only, not 100% tested.

Figure 14. Reset/Block Temporary Unprotect AC Waveforms

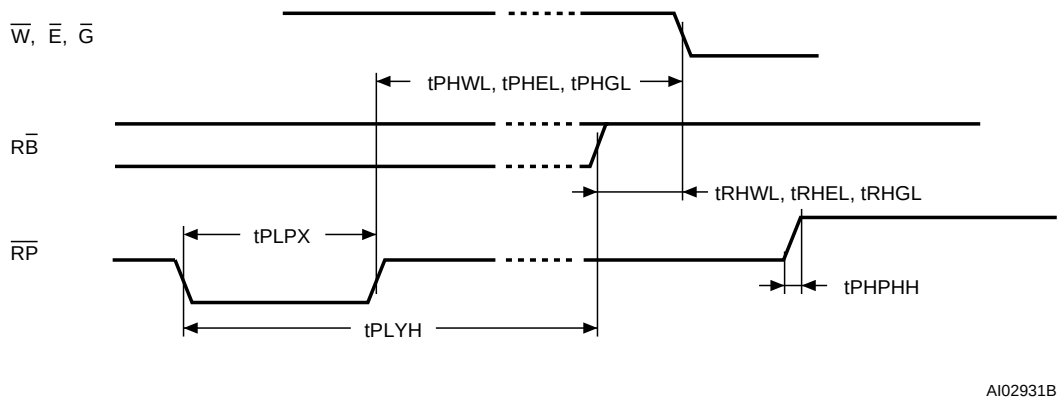
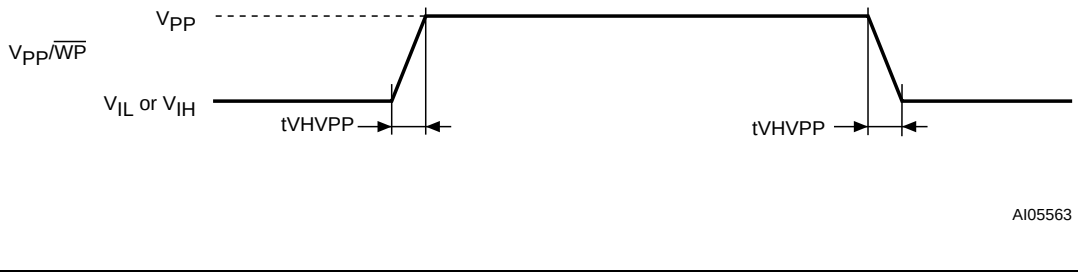


Table 16. Reset/Block Temporary Unprotect AC Characteristics

Symbol	Alt	Parameter		M29DW324D		Unit
				70	90	
t_{PHWL} (1) t_{PHEL} t_{PHGL} (1)	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL} (1) t_{RHEL} (1) t_{RHGL} (1)	t_{RB}	$R\overline{B}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	$\overline{RP}$ Pulse Width	Min	500	500	ns
t_{PLYH}	t_{READY}	$\overline{RP}$ Low to Read Mode	Max	50	50	µs
t_{PHPHH} (1)	t_{VIDR}	$\overline{RP}$ Rise Time to V_{ID}	Min	500	500	ns
t_{VHVPP} (1)		V_{PP} Rise and Fall Time	Min	250	250	ns

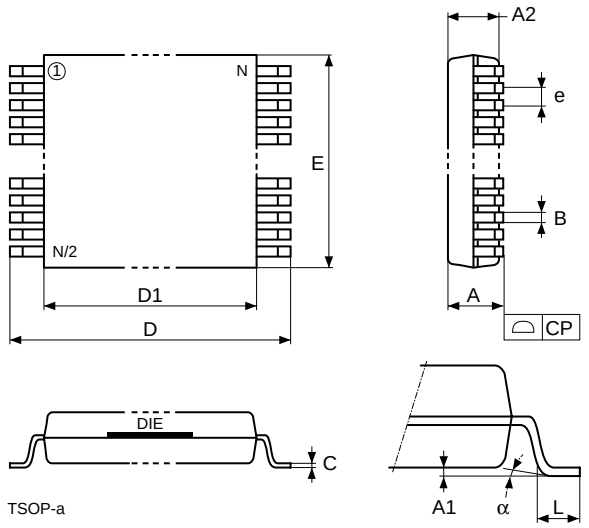
Note: 1. Sampled only, not 100% tested.

Figure 15. Accelerated Program Timing Waveforms



PACKAGE MECHANICAL

TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

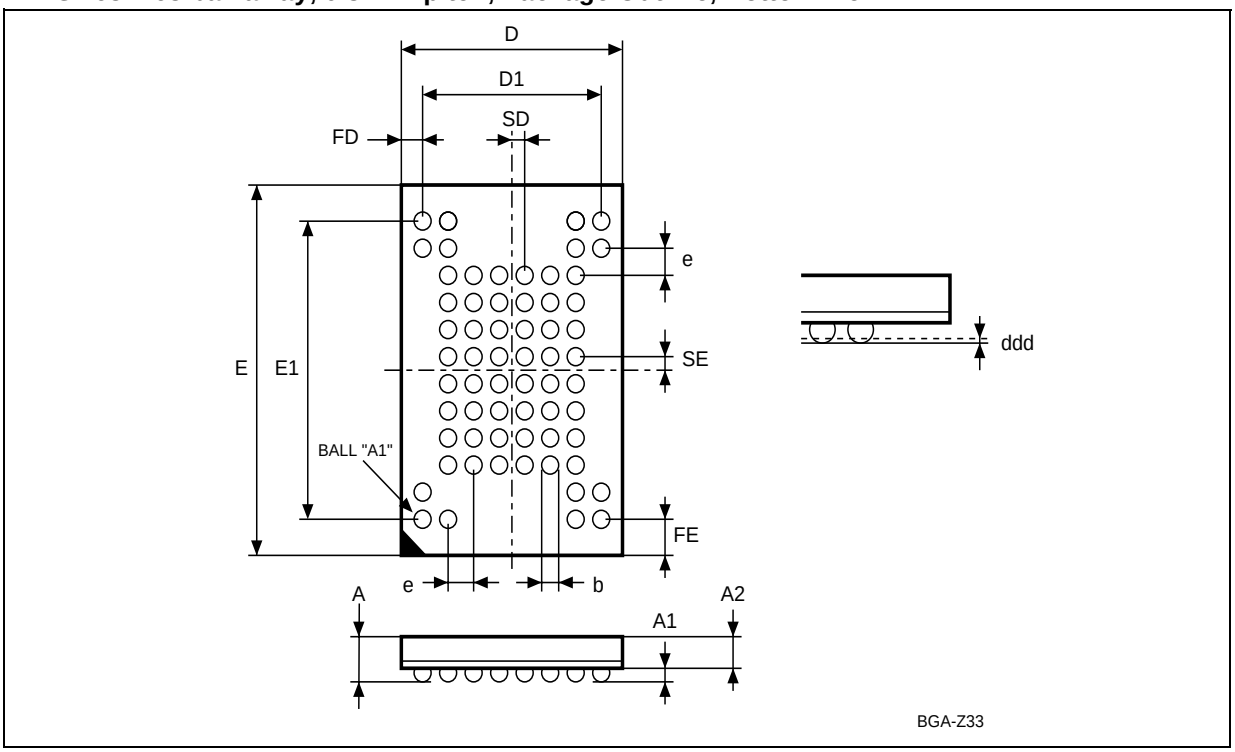


Note: Drawing is not to scale.

TSOP48 – 48 lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		11.90	12.10		0.4685	0.4764
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0279
α		0°	5°		0°	5°
N	48			48		
CP			0.10			0.0039

TFBGA63 – 63 ball array, 0.8 mm pitch, Package Outline, Bottom view



Note: Drawing is not to scale.

TFBGA63 – 63 ball array, 0.8 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.250			0.0098	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	7.000	6.900	7.100	0.2756	0.2717	0.2795
D1	5.600	–	–	0.2205	–	–
ddd	–	–	0.100	–	–	0.0039
E	11.000	10.900	11.100	0.4331	0.4291	0.4370
E1	8.800	–	–	0.3465	–	–
e	0.800	–	–	0.0315	–	–
FD	0.700	–	–	0.0276	–	–
FE	1.100	–	–	0.0433	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

PART NUMBERING

Table 17. Ordering Information Scheme

Example: M29DW324DB 70 N 1 T

Device Type
M29

Architecture
D = Dual Bank

Operating Voltage
W = V_{CC} = 2.7 to 3.6V

Device Function
324D = 32 Mbit (x8/x16), Boot Block, half-half partitioning

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
70 = 70 ns
90 = 90 ns

Package
N = TSOP48: 12 x 20 mm
ZA = FBGA63: 7x11mm, 0.80 mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

REVISION HISTORY

Table 18. Document Revision History

Date	Version	Revision Details
19-Apr-2002	-01	Document written

APPENDIX A. BLOCK ADDRESSES

Table 19. Top Boot Block Addresses, M29DW324DT

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank B	0	64/32	Protection Group	000000h–00FFFFh	000000h–07FFFh
	1	64/32	Protection Group	010000h–01FFFFh	008000h–0FFFFh
	2	64/32		020000h–02FFFFh	010000h–17FFFh
	3	64/32		030000h–03FFFFh	018000h–01FFFFh
	4	64/32	Protection Group	040000h–04FFFFh	020000h–027FFFh
	5	64/32		050000h–05FFFFh	028000h–02FFFFh
	6	64/32		060000h–06FFFFh	030000h–037FFFh
	7	64/32		070000h–07FFFFh	038000h–03FFFFh
	8	64/32	Protection Group	080000h–08FFFFh	040000h–047FFFh
	9	64/32		090000h–09FFFFh	048000h–04FFFFh
	10	64/32		0A0000h–0AFFFFh	050000h–057FFFh
	11	64/32		0B0000h–0BFFFFh	058000h–05FFFFh
	12	64/32	Protection Group	0C0000h–0CFFFFh	060000h–067FFFh
	13	64/32		0D0000h–0DFFFFh	068000h–06FFFFh
	14	64/32		0E0000h–0EFFFFh	070000h–077FFFh
	15	64/32		0F0000h–0FFFFFh	078000h–07FFFFh
	16	64/32	Protection Group	100000h–10FFFFh	080000h–087FFFh
	17	64/32		110000h–11FFFFh	088000h–08FFFFh
	18	64/32		120000h–12FFFFh	090000h–097FFFh
	19	64/32		130000h–13FFFFh	098000h–09FFFFh
	20	64/32	Protection Group	140000h–14FFFFh	0A0000h–0A7FFFh
	21	64/32		150000h–15FFFFh	0A8000h–0AFFFFh
	22	64/32		160000h–16FFFFh	0B0000h–0B7FFFh
	23	64/32		170000h–17FFFFh	0B8000h–0BFFFFh
	24	64/32	Protection Group	180000h–18FFFFh	0C0000h–0C7FFFh
	25	64/32		190000h–19FFFFh	0C8000h–0CFFFFh
	26	64/32		1A0000h–1AFFFFh	0D0000h–0D7FFFh
	27	64/32		1B0000h–1BFFFFh	0D8000h–0DFFFFh
	28	64/32	Protection Group	1C0000h–1CFFFFh	0E0000h–0E7FFFh
	29	64/32		1D0000h–1DFFFFh	0E8000h–0EFFFFh
	30	64/32		1E0000h–1EFFFFh	0F0000h–0F7FFFh
	31	64/32		1F0000h–1FFFFFh	0F8000h–0FFFFFh

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank A	32	64/32	Protection Group	200000h–20FFFFh	100000h–107FFFh
	33	64/32		210000h–21FFFFh	108000h–10FFFFh
	34	64/32		220000h–22FFFFh	110000h–117FFFh
	35	64/32		230000h–23FFFFh	118000h–11FFFFh
	36	64/32	Protection Group	240000h–24FFFFh	120000h–127FFFh
	37	64/32		250000h–25FFFFh	128000h–12FFFFh
	38	64/32		260000h–26FFFFh	130000h–137FFFh
	39	64/32		270000h–27FFFFh	138000h–13FFFFh
	40	64/32	Protection Group	280000h–28FFFFh	140000h–147FFFh
	41	64/32		290000h–29FFFFh	148000h–14FFFFh
	42	64/32		2A0000h–2AFFFFh	150000h–157FFFh
	43	64/32		2B0000h–2BFFFFh	158000h–15FFFFh
	44	64/32	Protection Group	2C0000h–2CFFFFh	160000h–167FFFh
	45	64/32		2D0000h–2DFFFFh	168000h–16FFFFh
	46	64/32		2E0000h–2EFFFFh	170000h–177FFFh
	47	64/32		2F0000h–2FFFFFh	178000h–17FFFFh
	48	64/32	Protection Group	300000h–30FFFFh	180000h–187FFFh
	49	64/32		310000h–31FFFFh	188000h–18FFFFh
	50	64/32		320000h–32FFFFh	190000h–197FFFh
	51	64/32		330000h–33FFFFh	198000h–19FFFFh
	52	64/32	Protection Group	340000h–34FFFFh	1A0000h–1A7FFFh
	53	64/32		350000h–35FFFFh	1A8000h–1AFFFFh
	54	64/32		360000h–36FFFFh	1B0000h–1B7FFFh
	55	64/32		370000h–37FFFFh	1B8000h–1BFFFFh
	56	64/32	Protection Group	380000h–38FFFFh	1C0000h–1C7FFFh
	57	64/32		390000h–39FFFFh	1C8000h–1CFFFFh
	58	64/32		3A0000h–3AFFFFh	1D0000h–1D7FFFh
	59	64/32		3B0000h–3BFFFFh	1D8000h–1DFFFFh
	60	64/32	Protection Group	3C0000h–3CFFFFh	1E0000h–1E7FFFh
	61	64/32		3D0000h–3DFFFFh	1E8000h–1EFFFFh
	62	64/32		3E0000h–3EFFFFh	1F0000h–1F7FFFh

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank A	63	8/4	Protection Group	3F0000h–3F1FFFh(1)	1F8000h–1F8FFFh(1)
	64	8/4	Protection Group	3F2000h–3F3FFFh(1)	1F9000h–1F9FFFh(1)
	65	8/4	Protection Group	3F4000h–3F5FFFh(1)	1FA000h–1FAFFFh(1)
	66	8/4	Protection Group	3F6000h–3F7FFFh(1)	1FB000h–1FBFFFh(1)
	67	8/4	Protection Group	3F8000h–3F9FFFh(1)	1FC000h–1FCFFFh(1)
	68	8/4	Protection Group	3FA000h–3FBFFFh(1)	1FD000h–1FDFFFh(1)
	69	8/4	Protection Group	3FC000h–3FDFFFh(1)	1FE000h–1FEFFFh(1)
	70	8/4	Protection Group	3FE000h–3FFFFFh(1)	1FF000h–1FFFFFh(1)

Note: 1. Used as the Extended Block Addresses in Extended Block mode.

Table 20. Bottom Boot Block Addresses, M29DW324DB

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank A	0	8/4	Protection Group	000000h-001FFFh(1)	000000h–000FFFh(1)
	1	8/4	Protection Group	002000h-003FFFh(1)	001000h–001FFFh(1)
	2	8/4	Protection Group	004000h-005FFFh(1)	002000h–002FFFh(1)
	3	8/4	Protection Group	006000h-007FFFh(1)	003000h–003FFFh(1)
	4	8/4	Protection Group	008000h-009FFFh(1)	004000h–004FFFh(1)
	5	8/4	Protection Group	00A000h-00BFFFh(1)	005000h–005FFFh(1)
	6	8/4	Protection Group	00C000h-00DFFFh(1)	006000h–006FFFh(1)
	7	8/4	Protection Group	00E000h-00FFFFh(1)	007000h–007FFFh(1)
	8	64/32	Protection Group	010000h-01FFFFh	008000h–00FFFFh
	9	64/32		020000h-02FFFFh	010000h–017FFFh
	10	64/32		030000h-03FFFFh	018000h–01FFFFh
	11	64/32	Protection Group	040000h-04FFFFh	020000h–027FFFh
	12	64/32		050000h-05FFFFh	028000h–02FFFFh
	13	64/32		060000h-06FFFFh	030000h–037FFFh
	14	64/32		070000h-07FFFFh	038000h–03FFFFh
	15	64/32	Protection Group	080000h-08FFFFh	040000h–047FFFh
	16	64/32		090000h-09FFFFh	048000h–04FFFFh
	17	64/32		0A0000h-0AFFFFh	050000h–057FFFh
	18	64/32		0B0000h-0BFFFFh	058000h–05FFFFh
	19	64/32	Protection Group	0C0000h-0CFFFFh	060000h–067FFFh
	20	64/32		0D0000h-0DFFFFh	068000h–06FFFFh
	21	64/32		0E0000h-0EFFFFh	070000h–077FFFh
	22	64/32		0F0000h-0FFFFFh	078000h–07FFFFh
	23	64/32	Protection Group	100000h-10FFFFh	080000h–087FFFh
	24	64/32		110000h-11FFFFh	088000h–08FFFFh
	25	64/32		120000h-12FFFFh	090000h–097FFFh
	26	64/32		130000h-13FFFFh	098000h–09FFFFh
	27	64/32	Protection Group	140000h-14FFFFh	0A0000h–0A7FFFh
	28	64/32		150000h-15FFFFh	0A8000h–0AFFFFh
	29	64/32		160000h-16FFFFh	0B0000h–0B7FFFh
	30	64/32		170000h-17FFFFh	0B8000h–0BFFFFh

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank A	31	64/32	Protection Group	180000h-18FFFFh	0C0000h–0C7FFFh
	32	64/32		190000h-19FFFFh	0C8000h–0CFFFFh
	33	64/32		1A0000h-1AFFFFh	0D0000h–0D7FFFh
	34	64/32		1B0000h-1BFFFFh	0D8000h–0DFFFFh
	35	64/32	Protection Group	1C0000h-1CFFFFh	0E0000h–0E7FFFh
	36	64/32		1D0000h-1DFFFFh	0E8000h–0EFFFFh
	37	64/32		1E0000h-1EFFFFh	0F0000h–0F7FFFh
	38	64/32		1F0000h-1FFFFFh	0F8000h–0FFFFFh
Bank B	39	64/32	Protection Group	200000h-20FFFFh	100000h–107FFFh
	40	64/32		210000h-21FFFFh	108000h–10FFFFh
	41	64/32		220000h-22FFFFh	110000h–117FFFh
	42	64/32		230000h-23FFFFh	118000h–11FFFFh
	43	64/32	Protection Group	240000h-24FFFFh	120000h–127FFFh
	44	64/32		250000h-25FFFFh	128000h–12FFFFh
	45	64/32		260000h-26FFFFh	130000h–137FFFh
	46	64/32		270000h-27FFFFh	138000h–13FFFFh
	47	64/32	Protection Group	280000h-28FFFFh	140000h–147FFFh
	48	64/32		290000h-29FFFFh	148000h–14FFFFh
	49	64/32		2A0000h-2AFFFFh	150000h–157FFFh
	50	64/32		2B0000h-2BFFFFh	158000h–15FFFFh
	51	64/32	Protection Group	2C0000h-2CFFFFh	160000h–167FFFh
	52	64/32		2D0000h-2DFFFFh	168000h–16FFFFh
	53	64/32		2E0000h-2EFFFFh	170000h–177FFFh
	54	64/32		2F0000h-2FFFFFh	178000h–17FFFFh
	55	64/32	Protection Group	300000h-30FFFFh	180000h–187FFFh
	56	64/32		310000h-31FFFFh	188000h–18FFFFh
	57	64/32		320000h-32FFFFh	190000h–197FFFh
	58	64/32		330000h-33FFFFh	198000h–19FFFFh
	59	64/32	Protection Group	340000h-34FFFFh	1A0000h–1A7FFFh
	60	64/32		350000h-35FFFFh	1A8000h–1AFFFFh
	61	64/32		360000h-36FFFFh	1B0000h–1B7FFFh
	62	64/32		370000h-37FFFFh	1B8000h–1BFFFFh

Bank	Block	(Kbytes/ Kwords)	Protection Block Group	(x8)	(x16)
Bank B	63	64/32	Protection Group	380000h-38FFFFh	1C0000h–1C7FFFh
	64	64/32		390000h-39FFFFh	1C8000h–1CFFFFh
	65	64/32		3A0000h-3AFFFFh	1D0000h–1D7FFFh
	66	64/32		3B0000h-3BFFFFh	1D8000h–1DFFFFh
	67	64/32	Protection Group	3C0000h-3CFFFFh	1E0000h–1E7FFFh
	68	64/32		3D0000h-3DFFFFh	1E8000h–1EFFFFh
	69	64/32		3E0000h-3EFFFFh	1F0000h–1F7FFFh
	70	64/32	Protection Group	3F0000h-3FFFFFh	1F8000h–1FFFFFh

Note: 1. Used as the Extended Block Addresses in Extended Block mode.

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 21, 22, 23, 24, 25 and 26 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 26, Security Code area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST.

Table 21. Query Structure Overview

Address		Sub-section Name	Description
x16	x8		
10h	20h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	36h	System Interface Information	Device timing & voltage information
27h	4Eh	Device Geometry Definition	Flash device layout
40h	80h	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
61h	C2h	Security Code Area	64 bit unique device number

Note: Query data are always presented on the lowest order data outputs.

Table 22. CFI Query Identification String

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query Unique ASCII String "QRY"	“Q”
11h	22h	0052h		"R"
12h	24h	0059h		"Y"
13h	26h	0002h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for Primary Algorithm extended Query table (see Table 24)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for Alternate Algorithm extended Query table	NA
1Ah	34h	0000h		

Note: Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 23. CFI Query System Interface Information

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} Logic Supply Minimum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	2.7V
1Ch	38h	0036h	V_{CC} Logic Supply Maximum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	3.6V
1Dh	3Ah	00B5h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5V
1Eh	3Ch	00C5h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5V
1Fh	3Eh	0004h	Typical timeout per single byte/word program = 2^n µs	16µs
20h	40h	0000h	Typical timeout for minimum size write buffer program = 2^n µs	NA
21h	42h	000Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	44h	0000h	Typical timeout for full chip erase = 2^n ms	NA
23h	46h	0004h	Maximum timeout for byte/word program = 2^n times typical	256 µs
24h	48h	0000h	Maximum timeout for write buffer program = 2^n times typical	NA
25h	4Ah	0003h	Maximum timeout per individual block erase = 2^n times typical	8 s
26h	4Ch	0000h	Maximum timeout for chip erase = 2^n times typical	NA

Table 24. Device Geometry Definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0016h	Device Size = 2^n in number of bytes	4 MByte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface Code description	x8, x16 Async.
2Ah 2Bh	54h 56h	0000h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	NA
2Ch	58h	0002h	Number of Erase Block Regions. It specifies the number of regions containing contiguous Erase Blocks of the same size.	2
2Dh 2Eh	5Ah 5Ch	0007h 0000h	Region 1 Information Number of identical size erase block = 0007h+1	8
2Fh 30h	5Eh 60h	0020h 0000h	Region 1 Information Block size in Region 1 = 0020h * 256 byte	8Kbyte
31h 32h	62h 64h	003Eh 0000h	Region 2 Information Number of identical size erase block = 003Eh+1	63
33h 34h	66h 68h	0000h 0001h	Region 2 Information Block size in Region 2 = 0100h * 256 byte	64Kbyte

Note: The region information contained in addresses 2Dh to 34h (or 5Ah to 68h) is correct for the M29DW324DB. For the M29DW324DT the regions must be reversed.

Table 25. Primary Algorithm-Specific Extended Query Table

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0030h	Minor version number, ASCII	"0"
45h	8Ah	0000h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	8Ch	0002h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	8Eh	0001h	Block Protection 00 = not supported, x = number of sectors in per group	1
48h	90h	0001h	Temporary Block Unprotect 00 = not supported, 01 = supported	Yes
49h	92h	0004h	Block Protect /Unprotect 04 = M29W400B	4
4Ah	94h	0020h	Simultaneous Operations, x = number of blocks in Bank B	32
4Bh	96h	0000h	Burst Mode, 00 = not supported, 01 = supported	No
4Ch	98h	0000h	Page Mode, 00 = not supported, 01 = 4 page word, 02 = 8 page word	No
4Dh	9Ah	00B5h	V_{PP} Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5V
4Eh	9Ch	00C5h	V_{PP} Supply Maxmum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5V
4Fh	9Eh	000xh	Top/Bottom Boot Block Flag 02h = Bottom Boot device, 03h = Top Boot device	–

Table 26. Security Code Area

Address		Data	Description
x16	x8		
61h	C3h, C2h	XXXX	64 bit: unique device number
62h	C5h, C4h	XXXX	
63h	C7h, C6h	XXXX	
64h	C9h, C8h	XXXX	

APPENDIX C. BLOCK PROTECTION

Block protection can be used to prevent any operation from modifying the data stored in the memory. The blocks are protected in groups, refer to Appendix A, Tables 19 and 20 for details of the Protection Groups. Once protected, Program and Erase operations within the protected group fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

To protect the Extended Block issue the Enter Extended Block command and then use either the Programmer or In-System technique. Once protected issue the Exit Extended Block command to return to read mode. The Extended Block protection is irreversible, once protected the protection cannot be undone.

Programmer Technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a group of blocks follow the flowchart in Figure 16, Programmer Equipment Block Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all groups can be unprotected at the same time. To unprotect the chip follow Figure 17, Programmer Equipment Chip Unprotect Flowchart. Table 27, Programmer Technique Bus Operations, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

In-System Technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the memory has been fitted to the system.

To protect a group of blocks follow the flowchart in Figure 18, In-System Block Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all the groups can be unprotected at the same time. To unprotect the chip follow Figure 19, In-System Chip Unprotect Flowchart.

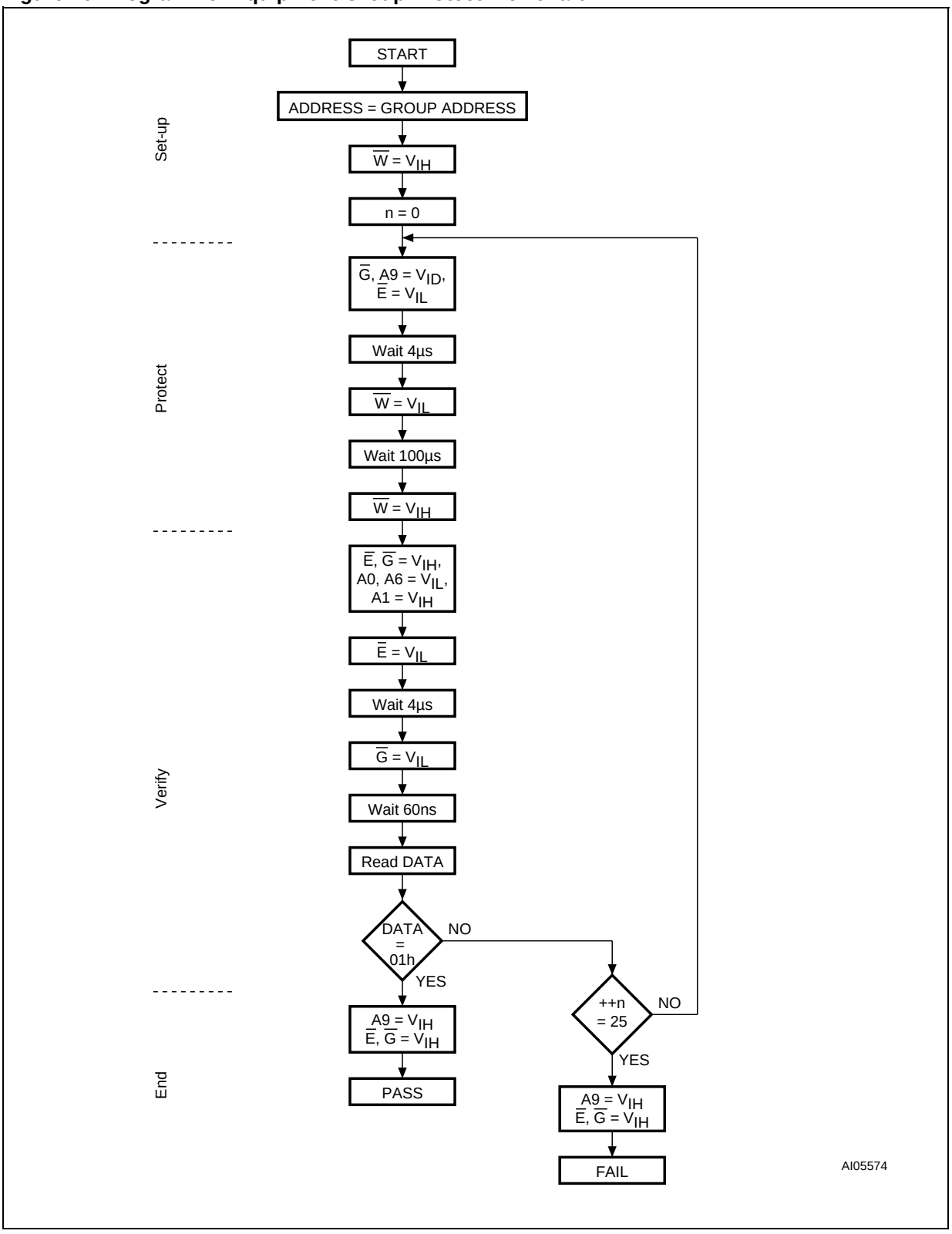
The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 27. Programmer Technique Bus Operations, $\overline{BYTE}$ = V_{IH} or V_{IL}

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A20	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Block (Group) Protect(1)	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-A20 Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others = X	X
Block (Group) Protection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A12-A20 Block Address Others = X	Pass = XX01h Retry = XX00h
Block (Group) Unprotection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A12-A20 Block Address Others = X	Retry = XX01h Pass = XX00h

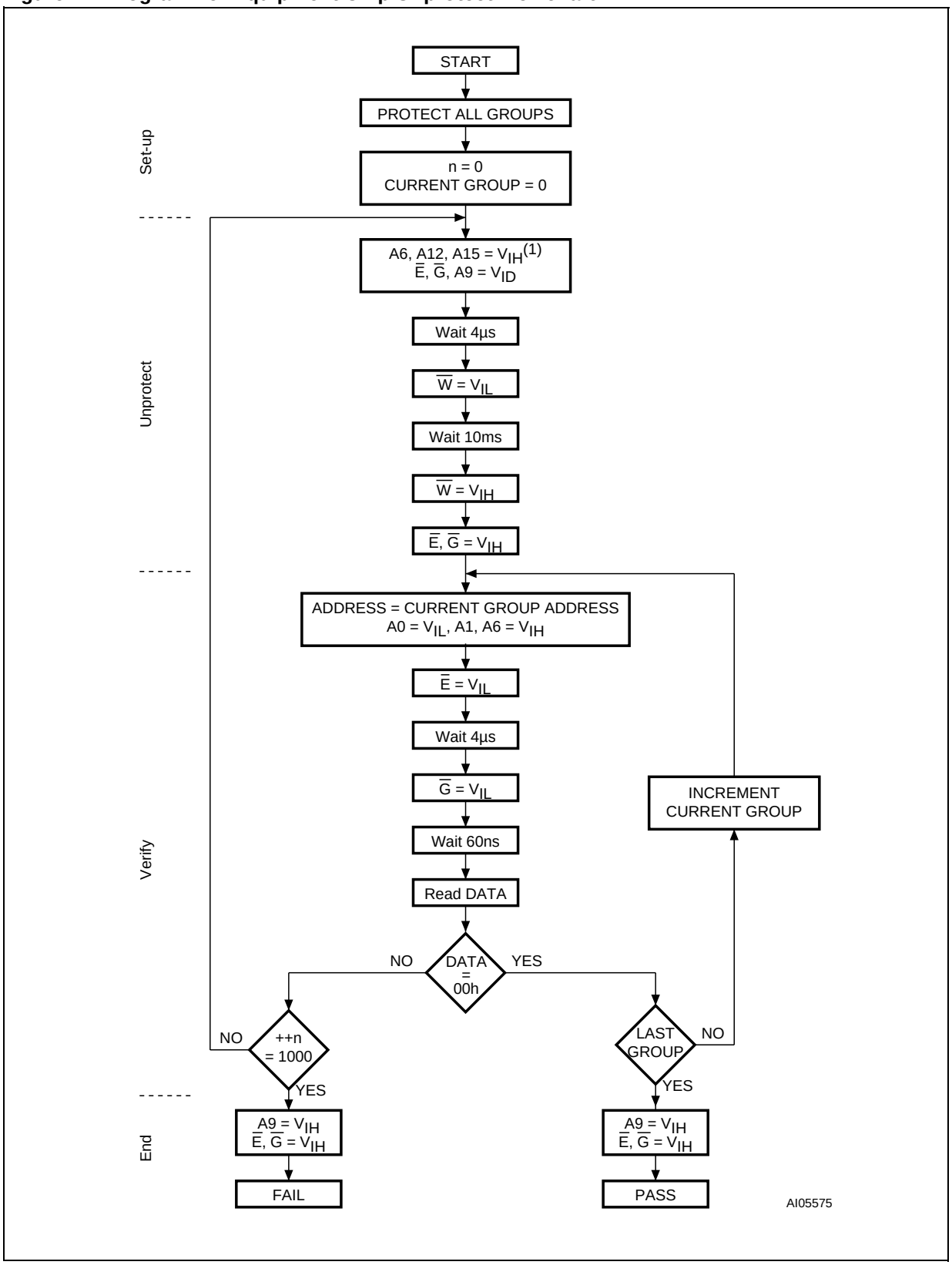
Note: 1. Block Protection Groups are shown in Appendix C, Tables 19 and 20.

Figure 16. Programmer Equipment Group Protect Flowchart



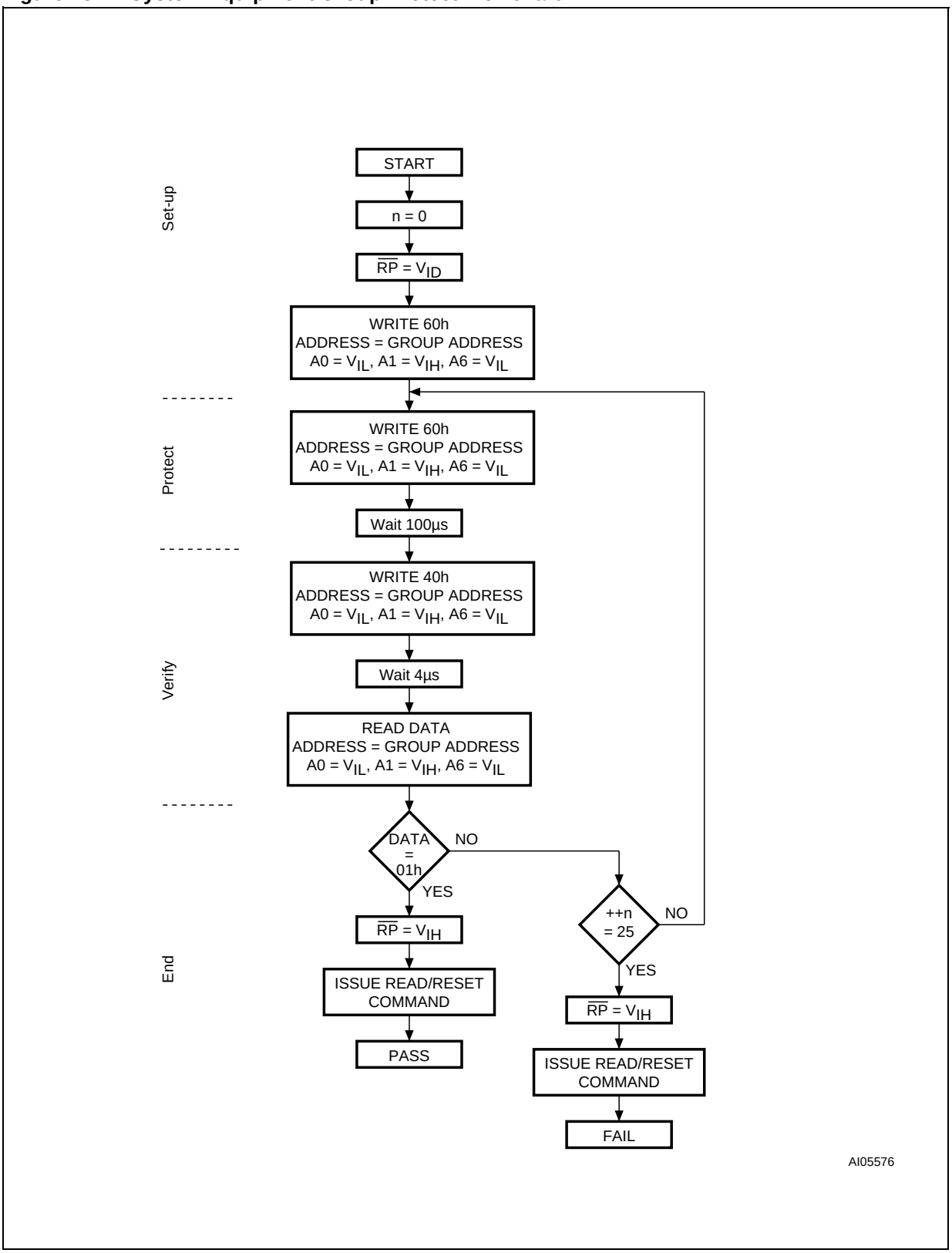
Note: Block Protection Groups are shown in Appendix C, Tables 19 and 20.

Figure 17. Programmer Equipment Chip Unprotect Flowchart



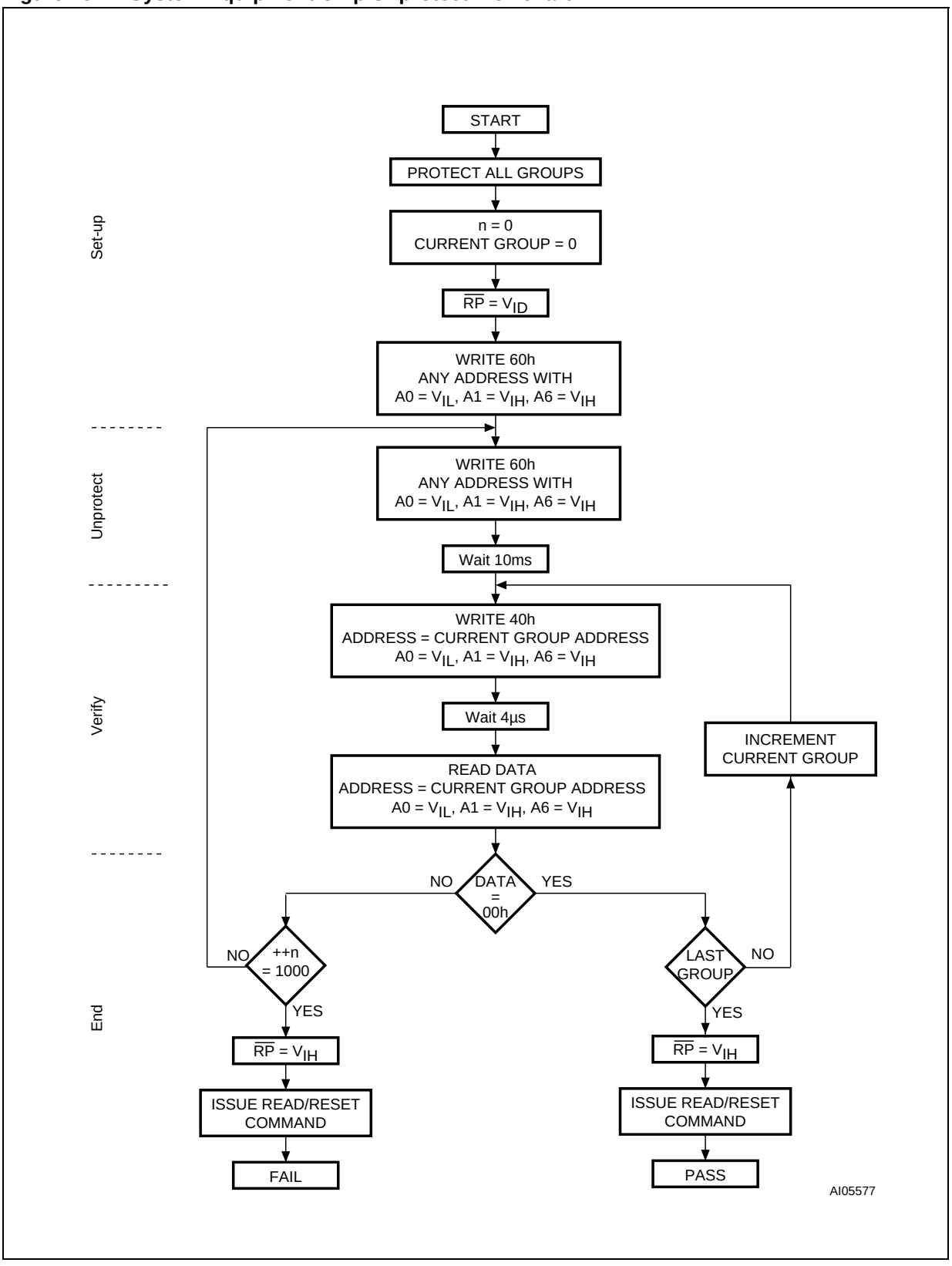
Note: Block Protection Groups are shown in Appendix C, Tables 19 and 20.

Figure 18. In-System Equipment Group Protect Flowchart



Note: Block Protection Groups are shown in Appendix C, Tables 19 and 20.

Figure 19. In-System Equipment Chip Unprotect Flowchart



Note: Block Protection Groups are shown in Appendix C, Tables 19 and 20.